FPGA Implementation of a Frame Synchronization Algorithm for Powerline Communications

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Abstract. *This paper presents an FPGA implementation of a pilot–based time synchronization scheme employing orthogonal frequency division multiplexing for powerline communication channels. The functionality of the algorithm is analyzed and tested over a real powerline residential network. For this purpose, an appropriate transmitter circuit, implemented by an FPGA, and suitable coupling circuits are constructed. The system has been developed using VHDL language on Nallatech XtremeDSP development kits. The communication system operates in the baseband up to 30 MHz. Measurements of the algorithm's good performance in terms of the number of detected frames and timing offset error are taken and compared to simulations of existing algorithms.*

Keywords

Field Programmable Gate Arrays (FPGAs), frequency division multiplexing, power line communications, frame synchronization.

1. Introduction

The use of indoor power lines to establish a residential network has gained rapid interest recently, following the demand for low–cost high speed data communications. Investigations have revealed that employing multicarrier modulation like orthogonal frequency division multiplexing (OFDM) can cope with the shortcomings of power lines as communication media [1]. In an OFDM system, synchronization at the receiver is a crucial issue. Failure in synchronization will result in increased inter–symbol and inter–carrier interference [2].

This paper describes a pilot–based method to achieve synchronization, tested for an OFDM–based system sending bursty data over the power line channel. The transmitter and the receiver are implemented digitally on field programmable gate array (FPGA) chips. Since the communication system operates in the baseband up to 30 MHz, the need for synchronization is limited to symbol timing, determining the beginning and end of an OFDM frame. The proposed synchronization method lies on the widely adopted Schmidl and Cox algorithm [3] for computing the frame start. The suggested modifications provide an algorithm with lower computational complexity and high system performance, when compared to existing algorithms.

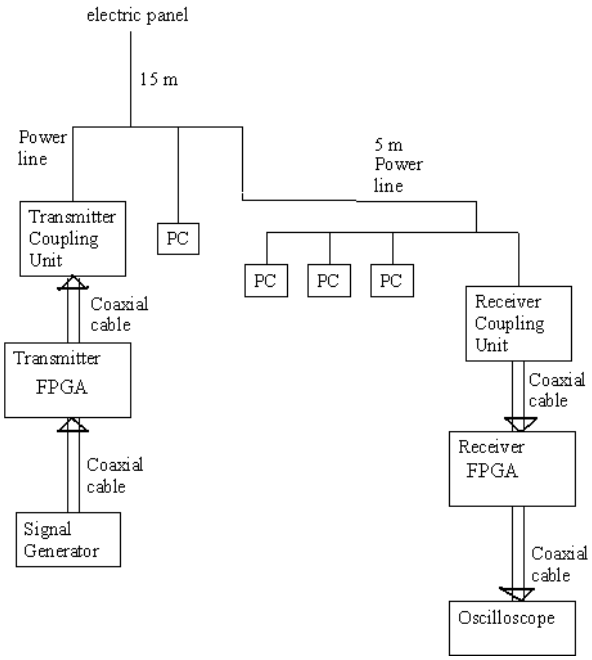

Fig. 1. The experimental setup where our OFDM system is tested.

2. OFDM System Analysis

Fig. 1 shows the experimental setup employed in order to test the synchronization algorithm over a real powerline channel. A signal generator that constitutes the source of input data is connected to the transmitter FPGA. The transmitter FPGA produces the modulated OFDM signal and passes it through a coaxial cable to the coupling unit. The transmitter coupling unit injects the OFDM signal into an F–type socket of a home powerline network. Through another socket of the home network, the receiver coupling unit extracts the OFDM signal and transfers it to the receiver FPGA. The receiver FPGA processes the received signal and depicts the synchronized frames on a digital oscilloscope.

The transmitter and the receiver lie on a distance of 5 m along a power line. Several PCs are also connected to the small home network topology as shown in Fig. 1.

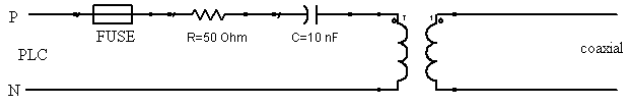

Fig. 2. Schematic diagram of the powerline coupling unit.

Fig. 2 presents the schematic diagram of the transmitter and receiver coupling device. The kernel of this apparatus consists of a wideband 1:1 transformer that isolates the power line and the communication circuits. The transformer's 1 dB bandwidth varies from 7 kHz to 80 MHz as long as both windings are terminated with a 50 Ω load. The primary winding consists of a 0.5A fuse for safety reasons, a 50 Ω resistor and a 10nF capacitor. Since the powerline network faces an impedance of a few Ohms, the resistor is used for impedance matching purposes, so that the primary's input impedance will not fall below 50 Ω in any case. The capacitor operates as a high pass filter that cuts off 50 Hz power voltage and noise below 1 MHz. The primary winding ends up to a C14 chassis socket. The secondary winding of the transformer is connected through a coaxial cable of 50 Ω characteristic impedance to a BNC type connector.

The transmitter and receiver FPGA have an analog voltage range of 4 V peak–to–peak. An analog–to–digital converter (ADC) of 105 MSPs sample rate at the input converts the analog signal to digital, 14–bit wide signal. The FPGA processes the digital signal at a clock rate of 105 MHz. A digital–to–analog converter (DAC) at the output of the FPGA converts the processed digital signal to analog. ADCs and DACs are terminated with a 50 Ω load at MCX type connectors.

The transmitter FPGA emits OFDM frames of constant length at normal time intervals. Two different OFDM architectures are adopted and are both tested over the powerline network.

The first architecture employs a simplified scheme where the available bandwidth is divided to 16 subcarriers. The subcarriers are loaded following binary phase shift keying (BPSK) so that the actual bandwidth lies in the region 4 – 22 MHz. Every sample lasts for 38 ns. In order to combat the multipath propagation effect, every transmitted symbol adopts a guard interval 4 samples long. A guard interval of 152 ns is sufficient for the tested network topology, since maximum delay spread longer than the adopted guard interval is not expected [4]. Every frame consists of 4 OFDM symbols of 20 samples each. The first two symbols are pilot, while the rest carry information data. The first training symbol is a sine waveform of frequency 13.16 MHz and is intended for frame synchronization at the receiver. Every frame lasts for 3040 ns and a new frame is emitted every 3952 ns. The maximum amplitude of the signal in every frame is 2 V. Fig. 3 depicts the emitted OFDM frames at the output of the transmitter.

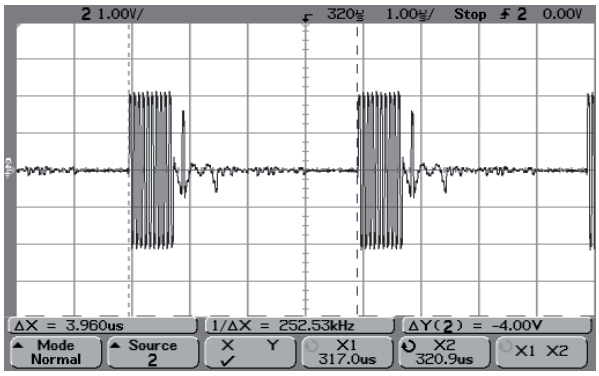

Fig. 3. OFDM frame at the output of the transmitter for the 16–carrier architecture.

The second architecture adopts a more complex scheme based on Homeplug BPL proposed by Homeplug Alliance for powerline communications [5]. The available bandwidth from 0 to 30 MHz is now divided to 1024 subcarriers. From those 1024 carriers, the 885 are usable leading to an actual bandwidth in the region 1.8 MHz to 24.5 MHz. The subcarriers are loaded following BPSK modulation. Every sample lasts for 38 ns. Homeplug BPL [6] employs various lengths for the guard interval (5.56 µs, 7.56 µs, 47.19 µs). We select a guard interval of 133 samples, namely 5.05 µs. Every frame consists of 4 OFDM symbols of 1157 samples each. Like the first architecture, the first two symbols are pilot, and the first symbol – intended for synchronization purposes – is a sine of frequency 13.16 MHz. Every frame lasts for 175.86 µs and a new frame is transmitted every 176.78 µs. Fig. 4 shows a screenshot of the OFDM frames at the output of the transmitter taken by a digital oscilloscope.

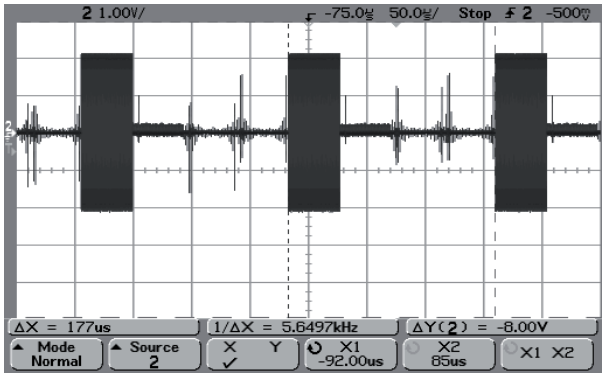

Fig. 4. OFDM frame at the output of the transmitter for the 1024 – carrier architecture.

The receiver FPGA implements the proposed synchronization algorithm described in the next section. The receiver FPGA should identify every arriving frame – distorted from the channel, extract the first pilot symbol, and output the remaining symbols of the frame.

3. Synchronization Algorithm

Our synchronization method is based on the timing offset estimation scheme proposed by Schmidl and Cox

[3]. The method requires a training symbol where the first half symbol – excluding the cyclic prefix – is identical to the second half. The sine pilot waveform of our OFDM system fulfils this property. Schmidl's algorithm uses a window of *2L* samples – where *L* the number of samples in one – half of the pilot symbol – that slides along in time as the receiver searches for the beginning of a new frame.

The algorithm is described by the following time metric:

$$M(d) = \frac{|R(d)|^2}{(S(d))^2} \tag{1}$$

where

$$R(d) = \sum_{m=0}^{L-1} r_{d+m}^{*} \cdot r_{d+m+L} \tag{2}$$

is the correlation between the received signal and its delayed by half a symbol version, and

$$S(d) = \sum_{m=0}^{L-1} |r_{d+m+L}|^2 \tag{3}$$

is the received energy for the second half symbol. The variable *d* is a time index corresponding to the first sample of the window.

When the training symbol has arrived, Schmidl's metric reaches a maximum indicating the frame synchronization point. However, the multiplications required to calculate Schmidl's metric, as described by (1) to (3), increase drastically the complexity of the algorithm making impossible to implement a high – speed FPGA design.

The proposed method uses a slithering window of *2L* samples, where a whole OFDM symbol can fit. Every sample is a 14–bit wide integer in two's complement representation, produced by sampling the analog OFDM signal. At every clock pulse, the window slides by one position, leaving the oldest sample out and importing the newest sample arriving from the ADC. At every pulse, the first *L* samples of the window are compared to the other *L* samples. The comparison includes an inverted exclusive–or operation so that the higher the resemblance between the compared samples, the higher value will face the outcome. An inverted exclusive–or operation is performed on a bit–by–bit basis, comparing the 14 bits of the first sample with the 14 bits of the other sample. The results of the comparisons, which are regarded as 14–bit positive integers, are then added. The adopted metric can be described formally by the expression:

$$M_1(d) = not\left(\sum_{m=0}^{L-1} r_{d+m} \oplus r_{d+m+L} \right) \tag{4}$$

where r_d is the sequence of the received signal samples. The variable *d* again is a time index corresponding to the first sample of the window. The sum is compared to a user defined threshold. If the sum exceeds the specified threshold, then synchronization has been found, otherwise the comparison window slides by one position at the next clock pulse and the search process is repeated. The level of the threshold is independent of the communication medium since channel distortions affect in more – or – less the same way the identical halves of the training symbol.

However, uniform background noise is likely to yield a high degree of resemblance between compared samples even if no actual signal is received. Thus, in order to avoid false synchronizations, the samples of the window are also compared to the *2L*–long sequence of the originally transmitted training symbol, which is a priori known to the receiver. The comparison is performed through an inverted exclusive–or operation as well. Formally, the adopted metric can be described as:

$$M_2(d) = not\left(\sum_{m=0}^{2L-1} r_{d+m} \oplus s_{d+m} \right) \tag{5}$$

where s_d is the sequence of the originally transmitted synchronization symbol. The results of the comparisons are added and the sum is compared to another threshold. The narrow bandwidth that the sine waveform occupies, leading to a minimal channel distortion, favors this pattern recognition algorithm. However, the communication medium is too severe for this method to stand alone. Thus, it is considered that synchronization has been found when both thresholds are exceeded simultaneously.

The length of every frame is fixed and a priori known to the receiver, so the synchronization algorithm need only identify the beginning of a frame. When synchronization has been found, the search process is suspended and the receiver outputs the remaining symbols of the frame just as they arrive. When the whole frame is exported, the search process for the next frame is resumed.

4. Results

The proposed synchronization algorithm is implemented on a Virtex IV FPGA. The design occupies 2670 slices. The implemented algorithm uses 3349 slice flip–flops and 4809 4-input LUTs. The design can operate up to a maximum frequency of 165 MHz.

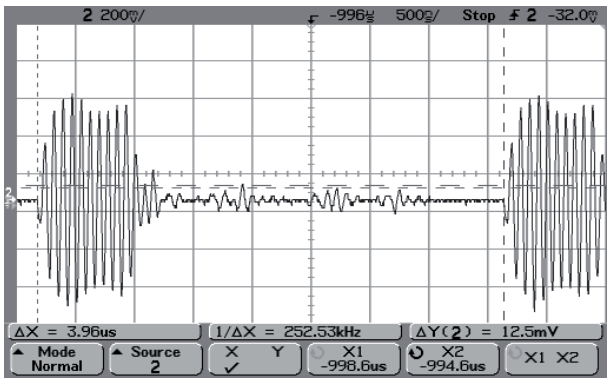

Fig. 5. Signal at the input of the receiver FPGA for the 16–carriers architecture.

Figs. 5 and 6 depict the performance of the synchronization scheme for the first OFDM architecture. Fig. 5 of the oscilloscope shows the arriving frames at the receiver, whereas Fig. 6 presents the frames synchronized following the proposed algorithm.

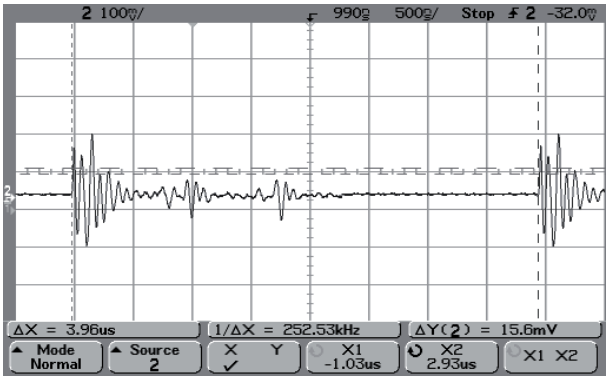

Fig. 6. Signal at the output of the receiver FPGA for the 16–carriers architecture.

Figs. 7 and 8 depict the arriving frames at the receiver and the synchronized frames, respectively, for the second OFDM architecture.

As shown in Figs. 6 and 8, the synchronization algorithm extracts with accuracy the first pilot symbol and outputs the remaining symbols of the frame. The distance between successive synchronized frames is 3.96 μs for the 16–carriers scheme and 177 μs for the 1024–carriers scheme, as expected.

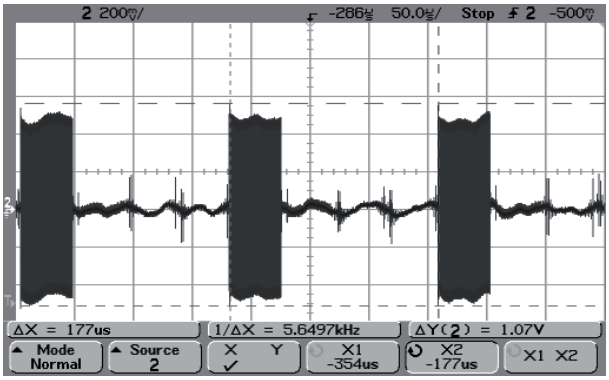

Fig. 7. Signal at the input of the receiver FPGA for the 1024–carriers architecture.

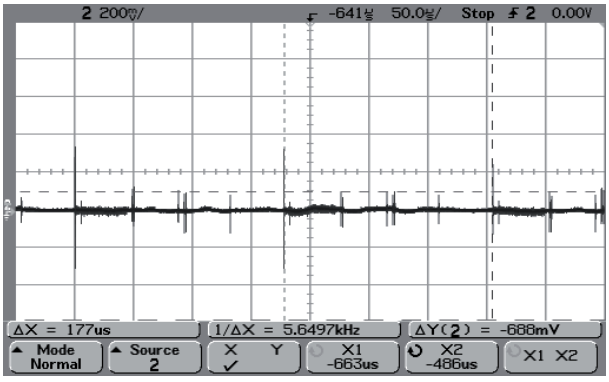

Fig. 8. Signal at the output of the receiver FPGA for the 1024–carriers architecture.

The noise that the power line network injects to the communication system has been measured around 100 mV – 200 mV. The synchronization signal at the input of the receiver has an amplitude of approximately 400 mV, as shown in Figs. 5 and 7, which corresponds to a signal–to–noise ratio of 6 – 12 dB. The amplitude of data symbols depends on the input data sequence at the transmitter, and can reach a peak value as high as the synchronization signal. For the specific data sequence employed by Figs. 5 to 8, the amplitude of the data symbols varies between 150 mV – 200 mV, which corresponds to a signal–to–noise ratio of 0 – 6 dB. Since the performance of the synchronization algorithm relies on the synchronization signal, it is considered that the algorithm is tested at a low signal–to–noise ratio of 6 – 12 dB.

Considering the OFDM architecture that the available bandwidth is divided to 16 carriers, the receiver FPGA recognizes 8190 frames in a time interval of 32.46 ms. This means that the receiver detects 99.7% of the frames emitted by the transmitter. Fig. 9 presents the timing offset per 100 detected frames at the receiver, which constitutes a measure of the accuracy that the exact point of synchronization is specified. As shown in Fig. 9, the error at the specification of the exact point of synchronization for the 16–carriers scheme is practically zero.

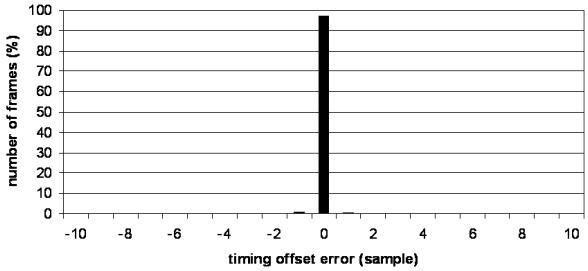

Fig. 9. Number of frames vs. timing offset for the 16–carriers scheme.

Regarding the 1024–carriers architecture, the receiver FPGA detects 8190 frames in a time interval of 1.453 s. Thus the receiver recognizes 99.6% of the transmitted frames. Fig. 10 shows the timing offset per 100 detected frames at the receiver and compares the timing offset performance of the proposed algorithm with that of the Schmidl's method.

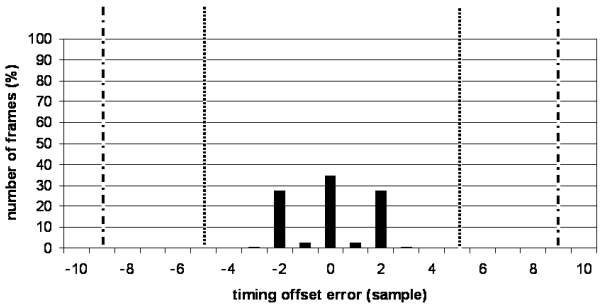

Fig. 10. Number of frames vs. timing offset for the 1024–carriers case. The dotted (dash–dotted) lines indicate the standard deviation of the Schmidl's method simulated over an AWGN (ISI) channel.

The dotted lines define the standard deviation of the timing offset for the Schmidl's method over an AWGN channel, as concluded from simulations [7]. The area defined by the dash–dotted lines indicates the standard deviation of the timing offset for the Schmidl's method simulated over an ISI channel [7]. As shown in Fig. 10, the maximum deviation of the timing offset for the proposed algorithm is only 3 samples, whereas the Schmidl's method faces a standard deviation of 5 samples over an AWGN channel and 9 samples over an ISI channel. Thus, the proposed method outperforms Schmidl's method for both AWGN and ISI channels.

5. Conclusion

A pilot–based frame synchronization scheme for an OFDM system intended for powerline communications has been presented. The algorithm has been realized digitally on FPGA chips and tested at a real environment. The proposed method is compared to Schmidl's method, offering significantly less computational complexity and much higher operation speed. Furthermore, the suggested algorithm has excellent performance regarding the number of detected frames and the accuracy of specifying the timing offset.

Acknowledgements

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